Docket No. 4425-343

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Chih-Yung Chen et al.	
Serial No.:	10/765,897	Examiner: DOAN, DUC T
Confirmation No:	2606	Group Art Unit: 2188
Filing Date:	January 29, 2004	
Title:	System Chip and Related Method of Data Access	

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPELLANT'S BRIEF UNDER 37 C.F.R. § 41. 37(C)

This brief is in furtherance of the Notice of Appeal, filed in this case on September 21, 2007.

The fees required under *§ 41.20* and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

Only one copy of this brief is required under *§ 41.37*.

This brief contains these items under the following headings, and in the order set forth below (*37 C.F.R. § 41.37(c)*):

I. Real Party in Interest.
II. Related Appeals and Interferences.
III. Status of Claims.
IV. Status of Amendments.
V. Summary of Claimed Subject Matter.
VI. Grounds of Rejection to be Reviewed on Appeal.
VII. Argument.
VIII. Claims Appendix.
IX. Evidence Appendix.
X. Related Proceedings Appendix.

I) REAL PARTY IN INTEREST

The real party in interest is VIA Technologies, Inc., located in Taipei, Taiwan, which is the assignee of this patent application.

II) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III) STATUS OF CLAIMS

Total Number of Claims in Application

There is a total of 20 claims in the application, which are identified as claims 1-20.

Status of all the claims

Claims cancelled: none

Claims withdrawn from consideration but not cancelled: none

Claims pending: claims 1-20

Claims allowed: none

Claims rejected: claims 1-20

Claims on Appeal

Claims on appeal are claims 1-20 as finally rejected by the Examiner.

IV) STATUS OF AMENDMENTS

No amendment after the final office action has been made.

V) SUMMARY OF CLAIMED SUBJECT MATTER

For the purpose of this appeal brief only, the claimed subject matter will be explained herein below with references to the specification by page and line number, and to the drawings by reference characters.

Independent **Claim 1** is directed to a data access apparatus (20, 21, 22, FIGs. 2A and 2B), comprising:

an external memory unit (21, FIGs. 2A and 2B) for storing data, wherein the external memory unit (21) has a second time cycle (302, FIG. 3) for performing a task;[1] and

a control unit (20, FIGs. 2A and 2B) coupled with the external memory unit (21) via a memory bus (22, FIGs. 2A and 2B),[2]

said control unit (20) comprising:

a microprocessor unit (201A, FIGs. 2A and 2B), having a first time cycle (304, FIG. 3) to perform a microprocessor operating;[3] and

a memory interface control unit (203, FIGs. 2A and 2B) for correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by the microprocessor unit (201A), into a data address of the external memory unit (21), thereby the microprocessor unit (201A) issuing the internal data access address could access data from the external memory unit (21) via the memory interface control unit (203);[4]

wherein

the external memory unit (21) has a data segment (210, FIG. 2B) storing flow control parameters and numerical arithmetic of the microprocessor unit (201A),[5] and

when the microprocessor unit (201A) attempts to access the data segment (210) storing flow control parameters and numerical arithmetic from the external

[1] See, for example, page 4, lines 25-26, and page 6, lines 18-19.
[2] See, for example, page 5, lines 9-10.
[3] See, for example, page 7, lines 23-24.
[4] See, for example, page 5, lines 10-16, page 6, lines 23-26, and page 7, lines 1-2.
[5] See, for example, page 5, lines 21-23.

memory unit (21), an access request signal (308, FIG. 3) issued from the control unit (20) associated with the microprocessor unit (201A) against another device accessing the external memory unit (21) is directed to the external memory unit (21), and the first time cycle (304) is suspended until an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[6]

Independent **Claim 8** is directed to a control unit (20, FIGs. 2A and 2B) for accessing data from an external memory unit (21, FIGs. 2A and 2B), having a second time cycle (302, FIG. 3), via a memory bus (22, FIGs. 2A and 2B) in an optical-electronic system,[7]

the control unit (20) comprising:

a microprocessor unit (201A, FIGs. 2A and 2B) having a first time cycle (304, FIG. 3) to perform a microprocessor operation;[8] and

a memory interface control unit (203, FIGs. 2A and 2B) for correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by the microprocessor unit (201A), into a data address of the external memory unit (21), thereby the microprocessor unit (201A) issuing the internal data access address could access data from the external memory unit (21) via the memory interface control unit (203);[9]

wherein

when the microprocessor unit (201A) attempts to access data from the external memory unit (21) via the memory interface, the control unit (20) is operable to send an access request signal (308, FIG. 3) to the external memory unit (21),[10]

flow control parameters and numerical arithmetic of the microprocessor unit (201A) is stored in a data segment (210, FIG. 2B) within the external memory unit (21),[11] and

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[6] See, for example, page 7, lines 11-24.
[7] See, for example, page 5, lines 9-10, and page 6, lines 18-19.
[8] See, for example, page 7, lines 23-24.
[9] See, for example, page 5, lines 10-16, page 6, lines 23-26, and page 7, lines 1-2.
[10] See, for example, page 7, lines 11-14.
[11] See, for example, page 5, lines 21-23.

when the microprocessor unit (201A) attempts to access the data segment (210) storing flow control parameters and numerical arithmetic from the external memory unit (21), the access request signal (308) issued from the control unit (20) associated with the microprocessor unit (201A) against another device accessing the external memory unit (21) is directed to the external memory unit (21), and the first time cycle (304) is suspended until an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[12]

Independent **Claim 15** is directed to a data access method used in a control unit (20, FIGs. 2A and 2B) for accessing data in an external memory unit (21, FIGs. 2A and 2B),[13]

said method comprising:

correspondingly transforming an internal data access address of an internal memory unit (202, FIGs. 2A and 2B), which is accessible only by a microprocessor unit (201A, FIGs. 2A and 2B) of the control unit (20), into a data address of the external memory unit (21), thereby the microprocessor (201A) issuing the internal data access address could access data from the external memory unit (21);[14]

suspending (400, FIG. 4) a first time clock (304, FIG. 3) used by the microprocessor (201A) of the control unit (20) when the microprocessor (201A) sends an access request signal (308, FIG. 3) for accessing a data segment (210, FIG. 2B) in the external memory unit (21), wherein the data segment (210) stores flow control parameters and numerical arithmetic of the microprocessor unit (201A), and wherein the access request signal (308) issued from the control unit (20) associated with the microprocessor unit (201A) against another device accessing the external memory unit (21) is directed to the external memory unit (21);[15] and

[12] See, for example, page 7, lines 11-24.
[13] See, for example, page 5, lines 12-14.
[14] See, for example, page 5, lines 10-16, and page 6, lines 23-26.
[15] See, for example, page 5, lines 21-23, page 7, lines 11-20, and page 9, lines 5-6.

reviving (406, FIG. 4) the first time clock (304) when an acknowledge signal (312, FIG. 3) indicating that the microprocessor unit (201A) may access the data segment (210) of the external memory unit (21) is received.[16]

[16] See, for example, page 7, lines 20-22, and page 9, lines 9-11.

VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3-8, 10-16 and 18-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Stoye* (USP 6,754,899) in view of *Fischer* (USP 6,438,672) and further in view of *Boudreau* (USP 4,493,036).

2. Claims 2, 9 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Stoye*, *Fischer*, *Boudreau* and in view of *Gappisch* (US 2003/0033490).

VII) ARGUMENT

Prior Art

Stoye

Stoye discloses a Share Memory Access Controller, in which (FIG. 1) a memory controller 16 is used to arbitrate between two competing processors IOP 11 and PP 12 accessing an external memory 15. See column 3, lines 57-62.

Fischer

According to the disclosure which Examiner relies upon, *Fischer* discloses in FIG. 6 a conventional cache controller 602 that monitors the address lines 605 to the processor 604, and then compares the address 605 with the address in the cache memory 603. If the cache hits, the cache memory 603 is accessed; otherwise, i.e., if the cache misses, the main memory 601 is accessed. See column 1, line 66 through column 2, line 13.

Boudreau

Boudreau discloses a data processing system, in which (FIG. 1) a priority resolver logic 108 is provided within a main memory 102 to resolve possible conflicts between competing requests (from I/O controller 103-106 or CPU 101) for access to RAM array 110. See column 1, lines 50-61.

Gappisch

Gappisch is directed to a non-volatile memory arrangement and method in a multiprocessor device. To reduce power consumption, the processor clock rates are varied depending on the current performance requirements. See Abstract.

Issues

Issue 1 - Whether Claims 1, 3-8, 10-16 and 18-20 Are Patentable Under 35 USC 103 Over *Stoye* in View of *Fischer* and further in view of *Boudreau*?

Issue 2 - Whether Claims 2, 9 and17 Are Patentable Under 35 USC 103 Over *Stoye*, *Fischer*, *Boudreau* and in view of *Gappisch*?

Arguments

Issue 1 - Whether Claims 1, 3-8, 10-16 and 18-20 Are Patentable Under 35 USC 103 Over Stoye in View of Fischer and further in view of Boudreau?

Claims 1, 3-8, 10-16 and 18-20

Claims 1, 3-8, 10-16 and 18-20 are patentable over *Stoye* in view of *Fischer* and further in view of *Boudreau* for at least the following reasons.[17]

With respect to one aspect of the claimed invention, the Examiner alleges that *Fischer* discloses the claimed "memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit ... into a data address of the external memory unit". See the last paragraph of page 4 through the first paragraph of page 5 of the Final Office Action. Appellant respectfully submits that *Fischer* does not disclose such claimed limitation, particularly, *Fischer* does not disclose that the memory interface control unit transforms the internal data access address into an external data address as claimed. Specifically, *Fischer* discloses (in FIG. 6 and column 1, line 66 through column 2, line 4) a cache controller 602 (considered by the Examiner to read on the claimed memory interface control unit) which **monitors** the address 605 issued by a processor 604 (considered by the Examiner to read on the claimed microprocessor unit), and then **compares** the address 605 with the address of a cache memory 603 (considered by the Examiner to read on the claimed internal memory unit). Accordingly, what is disclosed in *Fischer* is a cache controller 602 that monitors the

[17] To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. See *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The rule is obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

address of the processor 604 and compares the monitored address with the address of the cache memory 603. *Fischer* neither indicates nor mentions any "**transforming** an internal data access address of an internal memory unit ... into a data address of the external memory unit" as claimed.

A person of ordinary skill in the art would understand that "transform" means to change at least some characteristic of an object. In the claimed invention, the internal address of the internal memory unit is transformed into an external address of the external memory unit (by the memory interface control unit), i.e., not only the address is changed from an internal one to an external one, but the characteristic of the transformed address (for example, the numerical representation of the memory location) is also changed. On the contrary, in *Fischer*, the address 605 of the processor 604 is only monitored and then compared with the address of the cache memory 603. No form of address transformation is disclosed or suggested to occur when the *Fischer*'s system determines whether the cache hits or misses. Accordingly, a person skilled in the pertinent art would not have been motivated to transform an internal address into an external address based on the disclosure of *Fischer*.

With respect to another aspect of the claimed invention, the Examiner alleges in the second paragraph of page 3 of the Final Office Action that *Stoye* discloses (in FIG. 1) the claimed "control unit" (considered by the Examiner to correspond to IOP 11) and the claimed "microprocessor unit" (considered by the Examiner to correspond to PP 12). Examiner further alleges in the third paragraph of page 4 of the Final Office Action that *Stoye* further discloses the claimed "another device" (considered by the Examiner to correspond again to IOP 11), such that "an access request signal issued from the control unit ... against **another device** accessing the external memory unit" as claimed. Appellant respectfully disagrees with the Examiner's unreasonable reading of the references. Specifically, the Examiner improperly interprets a single element of *Stoye*, i.e., IOP 11, to read on different claim elements i.e., the claimed "control unit" and the claimed "another device" which compete for access to the external memory. A person of ordinary skill in the art would realize that the *Stoye* IOP 11 cannot be considered to compete for memory access against itself, and that the IOP 11 is readable at best only on one, not both, of the claimed "control unit" and the claimed "another device."

The above deficiencies are not curable by the teaching reference of *Boudreau* which is relied upon for another claim feature.

Accordingly, Appellant respectfully submits that the references are not combinable in the manner proposed by the Examiner and also fail to teach or suggest, singly or in combination, all features of the rejected claims. Claims 1, 3-8, 10-16 and 18-20 should therefore be considered patentable over the prior art references.

Issue 2 - Whether Claims 2, 9 and 17 Are Patentable Under 35 USC 103 Over Stoye, Fischer, Boudreau and in view of Gappisch?

Claims 2, 9 and 17

Dependent claims 2, 9 and 17 are patentable over *Stoye*, *Fischer*, *Boudreau* and in view of *Gappisch* for at least the same reasons advanced under Issue 1 with respect to the respective independent claims, as the deficiencies of *Stoye*, *Fischer* and *Boudreau* are not curable by *Gappisch*.

Claims 2, 9 and 17 should therefore be considered patentable over the prior art references.

CONCLUSION

In summary, appellant respectfully submits that claims 1-20 are patentable because the applied references singly or in combination fail to disclose, teach or suggest all limitations of the rejected claims, namely

1. *Fischer* and *Stoye* neither teach nor suggest the claimed feature "transforming an internal data access address of an internal memory unit ... into a data address of the external memory unit", and

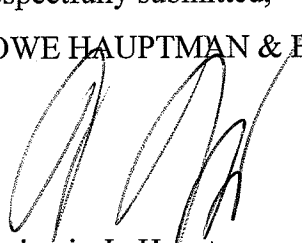
2. It is unreasonable to interpret a single element of *Stoye* to read on both claimed "control unit" and "another device" as recited in the independent claims, i.e., "an access request signal issued from the control unit ... against **another device** accessing the external memory unit".

Each of the Examiner's rejections has been traversed. Accordingly, Appellant respectfully submits that all claims on appeal are considered allowable. Reversal of the Examiner's Final Rejection is believed appropriate and courteously solicited.

If for any reason this Appeal Brief is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, Applicant's attorney of record.

Respectfully submitted,

LOWE HAUPTMAN & BERNER, LLP



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VIII) CLAIMS APPENDIX

1. A data access apparatus, comprising:

an external memory unit for storing data, wherein the external memory unit has a second time cycle for performing a task; and

a control unit coupled with the external memory unit via a memory bus, said control unit comprising:

a microprocessor unit, having a first time cycle to perform a microprocessor operating; and

a memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by the microprocessor unit, into a data address of the external memory unit, thereby the microprocessor unit issuing the internal data access address could access data from the external memory unit via the memory interface control unit;

wherein

the external memory unit has a data segment storing flow control parameters and numerical arithmetic of the microprocessor unit, and

when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, an access request signal issued from the control unit associated with the microprocessor unit against another device accessing the external memory unit is directed to the external memory unit, and the first time cycle is suspended until an acknowledge signal indicating that the microprocessor unit may access the data segment of the external memory unit is received.

2. The data access apparatus according to claim 1, wherein the first time cycle is longer than the second time cycle.

3. The data access apparatus according to claim 1, wherein the first time cycle is revived from suspending when the second time cycle is finished.

4. The data access apparatus according to claim 3, wherein the duration suspending the first time cycle is a time when the external memory unit finishes a current task.

5. The data access apparatus according to claim 1, wherein the external memory unit is a dynamic random access memory (DRAM).

6. The data access apparatus according to claim 1, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

7. The data access apparatus according to claim 1, wherein the data access apparatus could be applied to an optical-electronic system and which is selected from: a CD-ROM, CD-RW, DVD+/-ROM, DVD+/-RW.

8. A control unit for accessing data from an external memory unit, having a second time cycle, via a memory bus in an optical-electronic system, the control unit comprising:

a microprocessor unit having a first time cycle to perform a microprocessor operation; and

a memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by the microprocessor unit, into a data address of the external memory unit, thereby the microprocessor unit issuing the internal data access address could access data from the external memory unit via the memory interface control unit;

wherein

when the microprocessor unit attempts to access data from the external memory unit via the memory interface, the control unit is operable to send an access request signal to the external memory unit,

flow control parameters and numerical arithmetic of the microprocessor unit is stored in a data segment within the external memory unit, and

when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, the access

request signal issued from the control unit associated with the microprocessor unit against another device accessing the external memory unit is directed to the external memory unit, and the first time cycle is suspended until an acknowledge signal indicating that the microprocessor unit may access the data segment of the external memory unit is received.

9. The control unit of data access according to claim 8, wherein the first time cycle is longer than the second time cycle.

10. The control unit of data access according to claim 8, wherein the first time cycle is revived from suspending when the second time cycle is finished.

11. The control unit of data access according to claim 10, wherein the duration between the first time cycle suspended and revived is a time when the external memory unit finishes a current task.

12. The control unit of data access according to claim 8, wherein the external memory unit is a DRAM.

13. The control unit of data access according to claim 8, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

14. The control unit of data access according to claim 8, wherein the optical-electronic is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and DVD+/-RW.

15. A data access method used in a control unit for accessing data in an external memory unit, said method comprising:

correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by a microprocessor unit of the control unit, into a

data address of the external memory unit, thereby the microprocessor issuing the internal data access address could access data from the external memory unit;

suspending a first time clock used by the microprocessor of the control unit when the microprocessor sends an access request signal for accessing a data segment in the external memory unit, wherein the data segment stores flow control parameters and numerical arithmetic of the microprocessor unit, and wherein the access request signal issued from the control unit associated with the microprocessor unit against another device accessing the external memory unit is directed to the external memory unit; and

reviving the first time clock when an acknowledge signal indicating that the microprocessor unit may access the data segment of the external memory unit is received.

16. The data access method according to claim 15, wherein the external memory unit has a second time cycle which is a time for accessing data stored in the external memory unit.

17. The data access method according to claim 16, wherein the first time cycle is longer than the second time cycle.

18. The data access method according to claim 16, wherein duration of the first time cycle between being suspended and being revived is a time of the second time cycle being finished.

19. The data access method according to claim 15, further comprising the external memory unit performs a current task when suspending the first time cycle, and after finishing the current task, reviving the first time cycle immediately.

20. The data access method according to claim 15, wherein the method could be applied to an optical-electronic system which is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and a DVD+/-RW.

IX) EVIDENCE APPENDIX

None.

X) RELATED PROCEEDINGS APPENDIX

None.